ABSTRACT

A variable delay circuit includes a first delay circuit having a plurality of first delay stages connected in cascade. The first delay circuit receives an input signal at the initial stage of the first delay stages. A second delay circuit has a plurality of second delay stages identical to the first delay stages. The second delay circuit is connected in cascade and receives a first timing signal at the initial stage of the second delay stages. A detecting circuit receives a second timing signal asynchronous to the first timing signal, and detects, of delayed timing signals outputted from each of the second delay stages, a delayed timing signal having a transition edge near a transition edge of the second timing signal. A selecting circuit selects a delayed signal outputted from the first delay stage corresponding to the second delay stage outputting the delayed timing signal detected by the detecting circuit.